REMARKS

This application has been carefully reviewed in light of the Office Action mailed on September 9, 2003. Claims 1-2, 8-10, 18, 24-25, 27, 29-30, 32, 35, 37-38, 40-41, 44, 46, 48-49, 55-57, 62, 64, 68, 71-73, 76, 78-80, 87, 91, 94-96, 99, 101-103, 111, 113, 115-119, 123, and 125-127 have been amended. Claims 3-4, 11-12, 19-20, 26, 42-43, 47, 50-51, 58-59, 65-66, 69-70, 74-75, 81-82, 88-89, 92-93, 97, 104-105, 110, 112, 120-121, and 128-129 have been canceled. Claims 1-2, 5-10, 13-18, 21-25, 27-41, 44-46, 48-49, 52-57, 60-64, 67-68, 71-73, 76-80, 83-87, 90-91, 94-96, 98-103, 106-109, 111, 113-119, 122-127, 130-133 are now pending. Please reconsider the above-referenced application in light of the amendments and following remarks.

Figures 1 and 2 have been amended as required by the Office Action in Applicant's "Request for Approval of Proposed Drawing Amendments" filed concurrently herewith.

Claims 1-62 and 86-134 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly being non-enabled. The Office Action asserts that "the specification, while being enabling for passivation annealing process using deuterium, does not reasonably provide enablement for 'passivation process'." (Office Action, pg. 2). Moreover, that there "is insufficient guidance to enable one of ordinary skill in the art to determine which passivating species is selected for obtaining the advantage as recited in instant page 6, paragraph [0015]." (Office Action, pg. 2). Applicant respectfully disagrees.

Applicant's specification provides that a "passivating species for purposes of this invention, includes any species, such as deuterium, that are desirably provided so that the passivating species can occupy the trap sites in a semiconductor device." (Applicant's specification, pg. 8, paragraph 24). As a result, one of ordinary skill in the art would select a passivating species that occupies the trap sites in a semiconductor device. There is nothing unclear about this description, either in the specification or claims. Nonetheless, Applicant has amended claims 1-62 and 86-134 for clarification, and now claims 1-62 and

86-134 recite "a passivation process to passivate trap sites." Withdrawal of this rejection with regard to claims 1-62 and 86-134 is solicited.

Claims 1-10, 12-49, 51-62, 64-66, 72, 74, 80, 81, 87-90, 95, 97, 103, 105, 112, 113, 119, 121, 127 and 129 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. The claims have been amended to overcome the Examiner's concerns. Withdrawal of the rejection is respectfully submitted.

The Office Action states with respect to claim 1, line 6, "it is questioned what is recited through 'passivation process.' (Office Action, pg. 3). Applicant's specification provides that "the trap sites discussed previously can be passivated with different passivating species other than deuterium." (Applicant's specification, pg. 18, paragraph 53). As a result, a passivation process passivates trap sites with a passivating species. There is nothing unclear about this description, either in the specification or claims. Nonetheless, Applicant has amended claim 1 for clarification, and now claim 1 recites "a passivation process to passivate trap sites." Accordingly, withdrawal of the rejection is solicited.

The Office Action states with respect to claim 2, line 4 "it is questioned what is recited through the term 'negatively pulsing'." (Office Action, pg. 3). Negative pulses are generated in a gate bias waveform as a drain voltage is applied, i.e., a pulse of negative voltage (See Applicant's specification, pg. 15, paragraph 45). There is nothing unclear about this description, either in the specification or claims. Nonetheless, Applicant has amended claim 2 for clarification, and now claim 2 recites "said step of electrically stressing comprises applying a voltage potential to said drain while the gate is negatively pulsed." Accordingly, withdrawal of the rejection is solicited.

The Office Action states with respect to claim 20, "it is questioned what is recited through the term 'negative'." (Office Action, pg. 5). Negative pulses are generated in a gate bias waveform as a drain voltage is applied, i.e., a pulse of negative voltage (See Applicant's specification, pg. 15, paragraph 45). There is nothing unclear about this description, either in the specification or claims. Accordingly, withdrawal of the rejection is

solicited.

The Office Action states with respect to claims 20, 59, 82, 104 and 129 that "there is no description in the specification as originally filed of "generating negative pulses in a gate bias waveform." (Office Action, pg. 5). Applicant's specification provides that "[a] negative drain pulse is applied to the gate simply by generating negative pulses in the gate bias waveform as the drain voltage is applied." (Pg. 15, paragraph 45). There is nothing unclear about this description, either in the specification or claims. Nonetheless, claims 20, 59, 82, 104 and 129 have been canceled by the present Amendment to further expedite prosecution of the application. Accordingly, the rejection is now moot.

Claims 1-10, 12-19, 21 and 24 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ayadi in combination with Lyding. The rejection is respectfully traversed and reconsideration is requested in light of the current Amendment.

The Office Action asserts that Ayadi teaches "a process of stabilizing a semiconductor device . . . then electrically stressing the semiconductor device . . . to shorten the stress phase . . . and then identifying defective circuits so as the defective ones are not supplied as products." (March 14, 2003 Office Action, pg. 7) (emphasis added). Applicant respectfully submits that Ayadi and Applicant's claimed invention are completely different.

The cited references do not teach or suggest "a method for passivating trap sites in a semiconductor device, said method comprising fabricating a semiconductor device on a semiconductor substrate; electrically stressing the semiconductor device to remove non-passivating species from trap sites; and annealing said electrically stressed semiconductor device with a passivation process to passivate said trap sites," as recited in claim 1 (emphasis added).

Ayadi merely claims a method which shortens the stress phase of a semiconductor device that can identify shorted circuits. Ayadi does not teach or suggest

removing non-passivating species from trap sites and then annealing the semiconductor device to passivate the trap sites.

Lyding is relied upon for teaching "a method for treating or passivating [a] semiconductor device . . . by annealing [the] device with deuterium," (March 14, 2003 Office Action, pg. 7) and adds nothing to rectify the deficiencies associated with Ayadi. The Office Action alleges that Ayadi and Lyding are properly combinable since "it would enable the semiconductor device of Ayadi et al. to be performed and obtain further advantage of improving the operative characteristics of the device." (March 14, 2003 Office Action, pg. 7).

However, there is no motivation to combine these two references. Ayadi merely teaches that "the alternation of the second voltage increases the stress for the circuit configuration, so that the stressing time can be reduced and the same stress effect is achieved in a shorter time." (Col. 2, lines 54-57). In contrast, Lyding merely teaches the passivation of trap sites to resist aging (See Col. 3, lines 26-28). Ayadi is directed to locating shorted circuits so that the semiconductor device is not produced. Ayadi is not directed to prolonging or improving an operative semiconductor device.

Moreover, applying Ayadi's methods results in "the properties of a transistor [to] change as much in a few hours as in two years during normal operation." (Col. 2, lines 11-14). In other words, Ayadi teaches a method to age the semiconductor device in a short period of time. In contrast, Lyding teaches passivating trap sites with deuterium to prevent aging.

There is no teaching or suggestion in either reference to electrically stress a semiconductor device to remove non-passivating species from trap sites and anneal the electrically stressed device to passivate the trap sites. The Office Action contends that "the goals [of Ayadi and Lyding] are not incompatible because devices that passed the stress treatment of Ayadi et al. would usefully undergo the treatment of Lyding et al. to avoid further aging during use of the devices." (Office Action, pgs. 8-9). However,

incompatibility, even if true, does not mean that there is motivation in the references for combining their teachings.

Applicant respectfully submits that the Office Action has not set forth a *prima facie* case of obviousness. M.P.E.P. § 2144.03 provides that "[w]hen a rejection is based on facts within the personal knowledge of the examiner, the data should be stated as specifically as possible, and the facts must be supported." (emphasis added). There is no support for the Office Action's assertions, especially when the two cited references teach completely different processes: Ayadi prematurely ages the semiconductor device and Lyding seeks to prolong the age of the semiconductor device.

Moreover, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. § 2143.01 (emphasis added). In this case, the teachings of the cited references conflict with each other and there is no teaching or suggestion to combine Lyding's deuterium anneal with Ayadi's electrically stressed device.

Still further, Applicant respectfully submits that this is improper hindsight reconstruction. There is no teaching or suggestion in Ayadi that a subsequent process is needed to prevent aging when Ayadi teaches aging the device.

For at least these reasons, independent claim 1 is allowable over the cited references. Claims 2-6, 8, 9, 11-16, 18, 19, 21 and 24 depend from claim 1 and are similarly allowable.

Claims 23, 25-58, 60, 62-72, 74-81, 83, 85-95, 97-104, 106, 108-119, 121-128 and 130-134 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ayadi in combination with Lyding, and further in view of Applicant's Admitted Prior Art (AAPA). The rejection is respectfully traversed and reconsideration is requested.

Claims 23 and 25-39 depend from claim 1 and are similarly allowable for at least the reasons presented above with regard to claim 1. Primarily, Ayadi in combination with

Lyding does not teach or suggest "a method for passivating trap sites in a semiconductor device, said method comprising fabricating a semiconductor device on a semiconductor substrate; electrically stressing the semiconductor device to remove non-passivating species from trap sites; and annealing said electrically stressed semiconductor device with a passivation process to passivate said trap sites," as recited in claim 1. Applicant's admitted prior art is relied upon for teaching the formation of a semiconductor device and adds nothing to rectify the deficiencies associated with Ayadi and Lyding.

The cited references do not teach or suggest, "fabricating a transistor device on a silicon-on-insulator substrate, said transistor comprising a source, a gate, and a drain; electrically stressing said transistor to remove hydrogen occupying trap sites in the transistor; and annealing said electrically stressed transistor with a passivation process to passivate said trap sites," as recited in claim 40.

The cited references simply do not teach or suggest a process to remove hydrogen from trap sites by electrically stressing the device and then annealing the electrically stressed device with a passivation process to passivate trap sites. In addition, Lyding does not teach or suggest passivating a trap site after hydrogen is removed from the trap sites. Still further, the two references teach away from each other and are not properly combinable. Ayadi is directed to quickly aging a semiconductor device. In contrast, Lyding is directed to prevent aging of a semiconductor device. Claims 41-58, 60, and 62 depend from claim 40 and are similarly allowable along with claim 40.

The cited references do not teach or suggest "forming a transistor on a semiconductor substrate, said transistor having a source, a gate, a drain, and a plurality of trap sites, with hydrogen atoms occupying at least one of said trap sites; removing said at least one hydrogen atom from said trap sites; and providing deuterium atoms which bond to said trap sites after said at least one hydrogen atom is removed," as recited in claim 63.

The cited references simply do not teach or suggest a process to remove hydrogen from trap sites by electrically stressing the device and then providing deuterium

atoms to passivate the trap sites. In addition, Lyding does not teach or suggest passivating a trap site after hydrogen is removed from the trap sites. Still further, the two references teach away from each other and are not properly combinable. Ayadi is directed to quickly aging a semiconductor device. In contrast, Lyding is directed to prevent aging of a semiconductor device. Claims 64-72, 74-81, 83, and 85 depend from claim 63 and are similarly allowable along with claim 63.

The cited references do not teach or suggest "forming a transistor on a semiconductor substrate having a source, a gate, a drain, and a plurality of trap sites with non-passivating species occupying at least one of said trap sites, removing said at least one non-passivating species from said trap sites by electrically stressing said transistor; and providing at least one passivating species that occupies said trap sites," as recited in claim 86 (emphasis added).

The cited references simply do not teach or suggest a process to remove non-passivating species from trap sites by electrically stressing the transistor and then providing a passivating species to occupy the trap sites. Still further, the two references teach away from each other and are not properly combinable. Ayadi is directed to quickly aging a semiconductor device. In contrast, Lyding is directed to prevent aging of a semiconductor device. Claims 87-95, 97-104, 106, and 108-110 depend from claim 86 and are similarly allowable along with claim 86.

The cited references do not teach or suggest "forming a transistor having a plurality of trap sites, with non-passivating species occupying at least one of said trap sites, removing said at least one non-passivating species from the trap sites by electrically stressing the transistor, and providing at least one passivating species which bonds to said trap sites after said at least one non-passivating species is removed," as recited in claim 111.

Ayadi simply does not teach or suggest a process to remove non-passivating species from trap sites, nor does Lyding teach or suggest providing a passivating species at a to a trap site after a non-passivating species is removed. Moreover, the two references

teach away from each other and are not properly combinable. Ayadi is directed to quickly aging a semiconductor device. In contrast, Lyding is directed to prevent aging of a semiconductor device. Claims 112-119, 121-128 and 130-134 depend from claim 111 and are similarly allowable along with claim 111.

Claims 22, 61, 84, 107 and 131 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ayadi in combination with Lyding, and further in view of Applicant's Admitted Prior Art (AAPA), and further in view of Niimi. Reconsideration is respectfully requested.

Claim 22 depends from claim 1, claim 61 depends from claim 40, claims 84 and 107 depend from claim 63, and claim 131 depends from claim 111. For at least the reasons provided above with regards to claims 1, 40, 63 and 111, claims 22, 61, 84, 107 and 131 are similarly allowable. In particular, Ayadi does not teach or suggest a process to remove non-passivating species from trap sites, nor does Lyding teach or suggest providing a passivating species to a trap site after a non-passivating species is removed. Moreover, the two references teach away from each other and are not properly combinable. Ayadi is directed to quickly aging a semiconductor device. In contrast, Lyding is directed to prevent aging of a semiconductor device.

Niimi is relied upon for teaching a process for electrically stressing a semiconductor device at a temperature between 100 to 200°C and adds nothing to rectify the deficiencies associated with Ayadi and Lyding. Moreover, Applicant is claiming a passivation process that provides a passivating species at a temperature of less than about 650°C.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By_____

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